

buffer OR queue OR fifo "empty indicator"

- 2001

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All Results

Semi-synchronous dual port FIFO - group of 3 »

C Ryan

AJ Castellano - US Patent 5,555,524, 1996 - Google Patents

A Castellano

... In many cases, a FIFO memory serves 15 as a buffer between two portions of an electronic circuit ... 1, the FIFO 10 includes an empty indicator circuit 30 ...

A Williams

Cited by 35 - Related Articles - Web Search

V Nguyen E Chan

Cache memory command **buffer** circuit - group of 2 »

CP Ryan - US Patent 4,354,232, 1982 - Google Patents

... counter 214 and counter 215, and applies signals to write buffer storage memory ... of status signals utilized are as follows: (1) a full/empty indicator which is ...

Cited by 52 - Related Articles - Web Search

Asynchronous communications element - group of 3 »

MS Michael, PA Kanhere, RP Burnley, F Iacobelli, ... - US Patent 4,823,312, 1989 - Google

... A receiver time delay interrupt indicates to the CPU that there are data characters in the receiver FIFO which have not reached the ... RECEIVER BUFFER REGISTER 38 ... Cited by 51 - Related Articles - Web Search

Multi-processor, multi-bus system with bus interface comprising FIFO register stocks for receiving ... - group of 2 »

RJ Ternes, CA Huey, RW Bruner - US Patent 4,935,894, 1990 - Google Patents ... register 55 are ignored. Also, a predetermined number of lines in FIFO register stack 55 acts as a buffer. FIFO register stack 55 ...

Cited by 67 - Related Articles - Web Search

Instruction **buffer** associated with a cache memory unit - group of 2 » JE Wilhite, WA Shelly, CP Ryan - US Patent 4,521,850, 1985 - Google Patents ... In the preferred embodiment, types of status signals utilized are as follows: (1) a full/empty indicator which is a positive ... into the buffer to be useless. ... Cited by 24 - Related Articles - Web Search

Apparatus and method for asynchronous dual port FIFO - group of 3 » MT Kao, MM Chiang, MF Lin, WY Lin - US Patent 6,263,410, 2001 - Google Patents ... EMPTY INDICATOR CIRCUIT KA ... However, an extra buffer in the FIFO may be reserved for

defining an ALMOST FULL signal to prevent an error from occurring. ...

Cited by 14 - Related Articles - Web Search

FIFO buffer controller - group of 2 »

YA Geadah, MC Lefebvre - US Patent 4,873,667, 1989 - Google Patents ... [54] FIFO BUFFER CONTROLLER [75] Inventors: Youssef A. Geadah. Nepean: Martin C. Lefebvre, Ottawa, both ofCanada [73] Assignee: NorthernTelecom Limited ... Cited by 16 - Related Articles - Web Search

Intelligent stand-alone printfile buffer with paging control - group of 2 »

IY Houng - US Patent 4,630,198, 1986 - Google Patents
... [il] Patent Number: [45] Date of Patent: [54] INTELLIGENT STAND-ALONE PRINTFILE
BUFFER WITH PAGING ... 'f' the buffer i* capable of counting lines based upon ...

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Message FIFO buffer controller - group of 2 »

MC Lefebvre, CA Ciancibello, YA Geadah - US Patent 4,873,666, 1989 - Google Patents ... [54] [75] MESSAGE FIFO BUFFER CONTROLLER Inventors: Martin C. Lefebvre, Ottawa; Carmine A. Ciancibello; Youssef A. Geadah, both of Nepean, all of Canada [73 ... Cited by 27 - Related Articles - Web Search

Power-conservation system for computer peripherals - group of 3 » DJ Schanin, RR Billig - US Patent 5,477,476, 1995 - Google Patents ... Buffer 116 sets the "buffer empty" indicator negative; accordingly, controller 106 commands power switch 102 to turn on printer 108. ... Cited by 21 - Related Articles - Web Search

Data compression system with expansion protection - group of 3 » DJ Van Maren, JJ Kato - US Patent 4,870,415, 1989 - Google Patents ... data buffer is first to fill, the contents of the raw data buffer are to ... When no data is contained in a FIFO 13, 15, the respective empty indicator 141, 139 ... Cited by 18 - Related Articles - Web Search

... /write pointers independently selectable and simultaneously responsive to respective read/write FIFO ... - group of 3 »

DA Sherlock - US Patent 6,269,413, 2001 - Google Patents

... Shape Control with Baker 710/37 Queue Threshold Congestion ... of multiple logical FIFOs in **buffer** system 100 ... corresponds to the particular logical **FIFO** just read ... Cited by 13 - Related Articles - Web Search

Resynchronization of asynchronous transfer mode (ATM) switch fabric - group of 2 »

SS Merchant, MA Pashan, H Ueda, H Uematsu - US Patent 5,408,463, 1995 - Google Patents

 \dots corresponding queues, in the 60 114-N. Such **buffer** memory and \dots (Q)-empty comparator

105 and queue (Q)-emptyindica ... Q-empty comparator 107 and Q-empty indicator 108 ... Cited by 13 - Related Articles - Web Search

Buffered asynchronous communications element with receive/transmit control and status reporting - group of 4 »

MS Michael, PA Kanhere, RP Burnley, F Iacobelli, ... - US Patent 5,241,660, 1993 - Google Patents

... communications element includes a receiver shift register which receives serial data trans -fers from a communication station, a receiver FIFO which receives ... Cited by 10 - Related Articles - Web Search

Multi-processor data processing system peripheral equipment access units - group of 2 »

GJ Wisdom, PV Creteau, JL Williams - US Patent 4,041,460, 1977 - Google Patents ... register'soutput fill/empty indicator wheresuch indica- TheOUTPUT ACCEPTED signal notifies the queue This signal indicates the condition of the selected ... Cited by 7 - Related Articles - Web Search

Method and apparatus for synchronization between real-time sampled audio <u>applications operating full ...</u> - <u>group of 3 »</u> DF Strawn - US Patent 5,517,521, 1996 - Google Patents

... Areceive buffer, or FIFO, in the answer node is equipped 65 to generate ... indicatorand slows to F ^when the receive FIFO trips the Almost Empty indicator. ...

Cited by 9 - Related Articles - Web Search

Segmenting image data into blocks and deleting some prior to compression aroup of 2 »

GL Eldridge, F Blurfrushan, T Henning, SA Phong, ... - US Patent 6,272,252, 2001 - Google Patents

... The almost empty indicator must indicate when there is just one scanline in the FIFO. ... In all cases it is temporarily stored in a 16 line FIFO buffer 72 before ... Cited by 4 - Related Articles - Web Search

Highway transfer: a new packet forwarding technique for real-timeapplications T Kubo, K Yoguchi - INFOCOM'90. Ninth Annual Joint Conference of the IEEE ..., 1990 ieeexplore.ieee.org

... multiple input links contend for the link arid join a queue in the buffer; resulting in a ... long arid is divided into two parts; a full/empty indicator bit, FE ...

Cited by 3 - Related Articles - Web Search

Digital multiplexer for PCM voice channels having a cross-connect capability group of 3 »

HP Segal, C Dewilde - US Patent 4,685,101, 1987 - Google Patents

... (FOR DS0 EXTRACTION) S/P REGISTER |j BUFFER STORE II BUFFER STORE i; **TRANSMISSION**

ADDRESS BUS BUFFER EMPTY P/S REGISTER BUFFER STORE I BUFFER STORE ... Cited by 28 - Related Articles - Web Search

Digital carrier channel bus interface module for a multiplexer having a crossconnect bus system - group of 3 »

HP Segal, CA DeWilde - US Patent 4,697,262, 1987 - Google Patents

... 8B TRANSMISSION ADDRESS BUS RECEIVE ADDRESS BUS BUFFER EMPTY 16 -.TRANSMISSION DATA

BUS 16 ... Page 10. LINE INTERFACE SYNCHRONIZER S/P REGISTER n BUFFER STORE 1 ...

Cited by 18 - Related Articles - Web Search

High-speed modular switching apparatus for circuit and packet switched traffic - group of 2 »

H Ahmadi, JG Beha, WE Denzel, AP Engbersen, RP ... - US Patent 5,008,878, 1991 -**Google Patents**

... S OA GE FIFO STORAGE F A ,*7-/ LA I --> • 1TDM 1 J BUS :.. LINK *| 1R FROM r\rr*».r*i,r*

T-OUTPUT DCPACKCT - | (19-i) RPACKET FIFO | STORAGE (58 ADDR/CTL * ... Cited by 38 - Related Articles - Web Search

System and technique for synchronizing data to instructions in a real time computing application - group of 3 »

PG Rosen - US Patent 5,794,002, 1998 - Google Patents

... systems is to queue input data to the instruction ... the invention is implemented with a FIFO memory with an ... or the condition of the data buffer without departing ... Cited by 1 - Related Articles - Web Search

High speed digital data transmission by separately clocking and recombining interleaved data ... - group of 6 »

E Garcia, GS Lucas, JA Yanes - US Patent 6,091,783, 2000 - Google Patents ... Each buffer includes a data output line, a qualifier output line, and an empty indicator line. More particularly, the buffer 240 ...

Cited by 2 - Related Articles - Web Search

FIFO architecture with built-in intelligence for use in a graphics memory system for reducing paging ... - group of 3 » GW Reynolds - US Patent 6,150,679, 2000 - Google Patents

... the frame buffer memory to be device determines addresses in the first memory element for element which are eventually output from the FIFO memory BACKGROUND ... Cited by 6 - Related Articles - Web Search

Two cycle asynchronous FIFO queue - group of 6 »

TA Chu... - US Patent 5,550,780, 1996 - Google Patents

... 5,550,780 TWO CYCLE ASYNCHRONOUS FIFO QUEUE ... 1 shows in block diagram form aregister

stage of a two-cycle asynchronous FIFO queue according to the prior art. ...

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Foreword: Introduction and Issue Overview

K Kuemmerle, B Stuck, F Tobagi - Selected Areas in Communications, IEEE Journal on, 1983 - ieeexplore.ieee.org

... the slot. When the sender receives back the busy slot, it changes the full/empty indicator to empty. C. Buffer Insertion Ring In ... Related Articles - Web Search

An exact efficient discrete-event model for production lines withbuffers VS Kouikoglou, YA Phillis - Decision and Control, 1989., Proceedings of the 28th IEEE

1989 - ieeexplore.ieee.org

... The buffer—empty indicator is defined as follows (i, if B. empties at time t BE.(t) = LU, otherwise and similarly we define the following event indicators: BF ... Web Search

[сітатіол] High speed digital data transmission by separately clocking and recombining interleaved data ...

GS Lucas, JA Yanes, E Garcia - US Patent 6,246,726, 2001 Web Search

Local-Area Subnetworks: A Performance Comparison

BUX WERNER - IEEE TRANSACTIONS ON COMMUNICATIONS, 1981 ieeexplore.ieee.org

... packets is maximum if the probability that the packet joins an empty queue is as ... A full/empty indicator within the slot header is used to signal the state of a ... Related Articles - Web Search

One-to-many bus bridge using independently and simultaneously selectable logical FIFOS - group of 3 »

DA Sherlock - US Patent 6,304,936, 2001 - Google Patents ... and is dequeued from the second logical FIFO into the ... Control with Ray et al 710/52 Queue Threshold Congestion ... "Efficient Analysis of Shared Buffer " , & _ , _ ... Cited by 8 - Related Articles - Web Search

Design of a Network Shared Memory Based Workstation Cluster - group of 6

J Bonney, R Ramanujan, K Thurber - Proceedings of the 22nd Annual IEEE Conference on Local ..., 1997 - doi.ieeecomputersociety.org

... staggering or phasing of the full/empty indicator by one ... read operation until the transmit buffer is cleared ... newly updated data element from the receive FIFO. ... Related Articles - Web Search - BL Direct

Efficient point-to-point and multi-point routing mechanism for programmable packet switching nodes ... - group of 2 »

G Lebizay, JM Munier, A Pauporte, V Spagnol - US Patent 5,602,841, 1997 - Google Patents ... First, data packets are never copied, only packet pointers are copied for each destination: Space in **Buffer** Memory is saved, the number ofinstructions is ... Cited by 71 - Related Articles - Web Search

CACHE STORE CLEARING OPERATION FOR MULTIPROCESSOR MODE

RE Lange - US Patent 3,845,474, 1974 - Google Patents ... store 10 is a "look-aside memory" or high 10 speed **buffer** store. ... the present

embodiment

for providing a round robin counter and a full/empty indicator is shown ...

Cited by 52 - Related Articles - Web Search

Locking system for hotels - group of 2 »

J Schachter - US Patent 4,157,534, 1979 - Google Patents

... 5, 1979 Sheet 4 of 8 4,157,534 K EY CODE READ ER FI G. 6 FI G.10 VALI DATOR CIRCUITRY

FI FO MEMORY FIFO MEMORY -7¿ FRAM E T P U T RE GI S T ER 8 V p R G IE ...

Cited by 22 - Related Articles - Web Search

Parallel serial controller - group of 2 »

L Braun - US Patent 4,497,041, 1985 - Google Patents

... 72 - ?9 are connected to the PAO-PA7 inputs of FIFO incorporating microprocessors ... a single pulse; (i) said memory having a not **empty indicator** output connected ... Cited by 8 - Related Articles - Web Search

Method of interfacing peripheral devices with a central processor - group of 2

» . L Braun - US Patent 4,592,012, 1986 - Google Patents

... said memory output; providing said memory receiving means with a not-empty indicator in combination ... 72-79 are connected to the PAO-PA7 inputs of FIFO memory 81 ... Cited by 6 - Related Articles - Web Search

Method and apparatus for transporting messages between processors in a multiple processor system - group of 4 »

WT Futral, E Garbus, B Davis - US Patent 6,134,619, 2000 - Google Patents ... Stacy Whitmore Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman LLP [57] ABSTRACT Amessage unit that provides a hardware queue interface between a ... Cited by 27 - Related Articles - Web Search

Method of and apparatus for detecting toner empty - group of 2 » Y Yamaguchi, T Tooda - US Patent 5,512,980, 1996 - Google Patents

Page 1. United States Patent Yamaguchi et al. US005512980A [il] Patent Number: [45] Date of Patent: [54] METHOD OF AND APPARATUS FOR DETECTING TONER EMPTY ...

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<u>Programmable high performance data communication adapter for high speed</u> packet transmission networks - group of 3 »

C Galand, G Lebizay, D Mauduit, J Munier, A ... - US Patent 5,528,587, 1996 - Google Patents

... 18, 1996 IBM TDB, vol. 33, No. 7, pp. 351-354. Dec.A990 "Queue- ing problem avoidance by using finite resource list". Int. Conf. on ComputerDesign, 10-87, pp. ...

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Computer system including a write protection circuit for preventing illegal write operations and a ... - group of 3 »

DA Kummer, RT Rumer - US Patent 5,325,499, 1994 - Google Patents ... 9/1991 Begun et al 395/325 5,091,850 2/1992 Culley 395/400 5,157,774 10/1992 Culley

395/425 OTHER PUBLICATIONS "LR3220 Read-Write Buffer Preliminary," LSI ...

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[CITATION] Method and apparatus for transporting messages between processors in a multiple processor system

US Patent 5,925,099, 1999

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Image recording apparatus - group of 3 »

T Honjo, M Kitahara, Y Suzuki, N Takahata - US Patent 4,622,594, 1986 - Google Patents Page 1. United States Patent [il] Patent Number: Honjo et al [45] Date of Patent: [54] IMAGE RECORDING APPARATUS [75] Inventors: Takeshi ...

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<u>3D graphics in a single logical sreen display using multiple computer systems</u> US Patent 6,249,294, 2001 - freepatentsonline.com

... For example, a FIFO arrangement may ... request has the effect of clearing the colormap event queue in that ... The first few bytes of each buffer may be used as a full ... Cited by 7 - Related Articles - Cached - Web Search

MULT-PROCESSOR DATA PROCESSING SYSTEM

US Patent 3,787,818, 1974 - Google Patents

... SL Page 7. Y BUS PATENTEDJAN22 1974 3, 787, 8 1 8 SHEET 06 OF 1 3 MULTIPLEXOR QUEUE

SORTING CIRCUIT INTERFACE *EQUIPMENT * MULTIPLE XOR .TIMING CIRCUIT Page 8. ...

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Functional grammars - group of 2 »

VA Tuzov - Journal of Mathematical Sciences, 1983 - Springer

... <pair of boundaries >: : < boundary > [} I <empty indicator > ;

<lower bound > :: @ <m > [s] I <enqptyindicator> ; <empty ...</pre>

Related Articles - Web Search

Resource management system using next available integer from an integer pool and returning the ... - group of 3 »

GW Wilhelm Jr - US Patent 5,905,889, 1999 - Google Patents

... 1997 by GW Wilhelm, Jr. for Stationary Queue for Scarce * buffer) and the free _ii st variable is updated to point to the US patent application Ser. No. ...

Cited by 5 - Related Articles - Web Search

Resource management system having a control structure to indicate the availability of integer from ... - group of 3 »

GW Wilhelm Jr - US Patent 6,233,630, 2001 - Google Patents

... for Stationary Queue for Scarce Resource Management ... 2. The permission to use a resource

is a "ticket" for a specific resource only (ie, buffer #1, or program #5 ...

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Programmed controller - group of 3 »

D Ward, DB Steward - US Patent 4,802,116, 1989 - Google Patents Page 1. United States Patent Ward et al. [il] Patent Number: [45] Date of Patent: [54] PROGRAMMED CONTROLLER [75] Inventors: Derek ... Cited by 19 - Related Articles - Web Search

[BOOK] Sparse Distributed Memory Principles of Operation - group of 4 » MJ Flynn, P Kanerva, N Bhadkamkar - 1989 - historical.ncstrl.org Page 1. Sparse Distributed Memory: Principles and Operation MJ Flynn, P. Kanerva, and N. Bhadkamkar Technical Report CSL-TR-89-400 December 1989 ...

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Graphics memory system that utilizes look-ahead paging for reducing paging overhead - group of 3 »

GW Reynolds - US Patent 6,078,336, 2000 - Google Patents ... When the RAM controller is utilizing a particular FIFO to access the frame buffer memory, the RAM controller deter -mines when there are no more transactions ... Cited by 4 - Related Articles - Web Search

Image forming device - group of 2 »

Y Yamaguchi, H Hanzawa, S Tanaka, N Tanaka - US Patent 5,528,344, 1996 - Google **Patents**

... LESS) ? YES NEAR EMPTY (TONER EMPTY INDICATOR FLASHING) TONER ... YES **TONER EMPTY**

(TONER EMPTY INDICATOR LIGHTING, DEVICE NOT READY) TONER ...

Cited by 10 - Related Articles - Web Search

Graphics memory system that utilizes detached-Z buffering in conjunction with a batching ... - group of 6 »

GW Reynolds - US Patent 6,317,124, 2001 - Google Patents

... Z coordinate data is stored in the Z buffer storage area ... colors stored in the Write Pixel FIFO 81 will ... pixel colors until a write-pipe-empty indicator (not shown ...

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ELEMENT PLACEMENT SYSTEM

H Freitag - US Patent 3,654,615, 1972 - Google Patents Page 1. United States Patent Freitag [is] 3,654,615 [45] Apr. 4, 1972 [54] ELEMENT PLACEMENT SYSTEM [72] Inventor: Harlow Freitag ... Cited by 21 - Related Articles - Web Search

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